AMENDMENTS TO THE CLAIMS

Claims 1-9. (Cancelled)

10. (Previously Presented) The FET of claim 20, wherein said first conductive material is on a gate dielectric and said gate dielectric is on a substrate..

11. (Cancelled)

12. (Previously Presented) The FET of claim 20, wherein said first material comprises a first semiconductor material.

13. (Original) The FET of claim 12, wherein said first semiconductor material comprises germanium.

14. (Original) The FET of claim 12, wherein said first semiconductor material comprises a germanium compound Ge_xSi_{1-x}, wherein x is in the range of about 0.5 to about 1.0.

15. (Previously Presented) The FET of claim 20, wherein said second conductive material comprises polysilicon.

16. (Previously Presented) The FET of claim 20, wherein said first conductive material comprises polysilicon.

17. (Original) The FET of claim 16, wherein said second conductive material comprises a refractory metal.

18. (Original) The FET of claim 17, wherein said second conductive material comprises

tungsten, tantalum, molybdenum, or titanium.

19. (Previously Presented) The FET of claim 20, wherein said second conductive material comprises a silicide.

20. (Currently Amended) An FET, comprising a gate, said gate comprising first conductive material and a second conductive material different from said first conductive material, said second conductive material on said first conductive material, wherein said second conductive material extends beyond said first conductive material ~~by a given distance~~ to provide a T-shaped gate, ~~further wherein a thickness of said second conductive material is greater than a thickness of said first conductive material,~~ a first diffusion region self-aligned to the first conductive material, a second diffusion region defined by said second conductive material, ~~said first diffusion and said second diffusion regions being laterally offset by a distance equal to about said given distance;~~ and a spacer along sidewalls of said second conductive material, wherein a third implant is defined by said spacer, and further wherein an air gap is left behind said spacer along a notched sidewall of said first conductive material.

Claims 21-44. (Canceled)

45. (Previously Presented) The FET of claim 46, wherein said upper portion of said gate extends beyond said lower portion to provide a T-shaped gate.

46. (Currently Amended) An FET, comprising:

a gate disposed on a substrate, said gate comprising a lower portion having first sidewalls and an upper portion having second sidewalls, said first and second sidewalls being laterally offset~~, wherein a thickness of said second sidewalls is greater than a thickness of said first sidewalls~~;

spacers disposed on said second sidewalls and extending down to said substrate without contacting said first sidewalls to define an air gap therebetween;

a first implant disposed in said substrate and aligned to said first sidewalls; and

a second implant disposed in said substrate and aligned to said second sidewalls; ~~said first and second implant being offset by a distance equal to about said lateral offset of said first and second sidewalls~~.

47. (Previously Presented) The FET of claim 46, further comprising:

a third implant disposed in said substrate and aligned to said spacers.

48. (New) The FET of claim 20, wherein said first diffusion region comprises a first impurity having a first conductivity type and said second diffusion region comprises a second impurity having a second conductivity type.

49. (New) The FET of claim 48, wherein said third implant comprises said second impurity.

50. (New) The FET of claim 20, wherein a thickness of said second conductive material is greater than a thickness of said first conductive material.

51. (New) The FET of claim 20, wherein said first diffusion and said second diffusion regions are laterally offset by a distance equal to about a given distance that said second conductive material extends beyond said first conductive material.

52. (New) The FET of claim 46, wherein said first implant comprises a first impurity having a first conductivity type and said second implant comprises a second impurity having a second conductivity type.

53. (New) The FET of claim 46, wherein a thickness of said second sidewalls is greater than

a thickness of said first sidewalls.

54. (New) The FET of claim 46, wherein said first and second implant are offset by a distance equal to about said lateral offset of said first and second sidewalls.